IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Venkatesh Natarajan, et a

Serial No.:

09/451,979

Filed:

October 20, 1999

For:

TI-28917

Art Unit: 2823

Examiner: Julio J. Maldonado

Conf. No: 4880

A Method And Apparatus For Combining Memory Blocks For In Circuit Emulation

LETTER TO THE OFFICIAL DRAFTSPERSON

Ass't Commissioner for Patents

Washington, D.C. 20231

Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1 8(a) 3 I hereby certify that the above correspondence is being deposited with 4 the U.S. Postal Service as First Class Mail in an envelope addressed to Ass't Commissioner for Patents, Washington, D.C. 20231 on 2 April 8, 2003

Please find enclosed the formal drawings for the subject case. Charge any necessary fees to Texas Instruments Incorporated, Deposit Account No. 20-0668. This form is submitted in triplicate.

Respectfully submitted,

Gerald E. Laws

Attorney for Applicant

Reg. No. 39,268

Texas Instruments Incorporated P.O. Box 655474, MS 3999